520.43863X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. OHTA et al

Serial No.: 10/849,211

Filed: May 20, 2004

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

Group: 2815

Examiner: E. LEE

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
POB 1450
Alexandria, VA 22313-1450

November 7, 2005

Sir:

In reply to the Office Action, dated August 5, 2005, the period of response for which extension of time is requested in the attached Petition for Extension of Time, applicants hereby elect the Group I claims 1-9, drawn to a semiconductor device, *without traverse*. Applicants also hereby select Species 1 (Fig. 1), *with traverse*.

More specifically, applicants respectfully traverse the Election of Species Requirement due to the close relationship between the species of Figs. 1, 2, 5 and 7. Fig. 1 provides the first embodiment of the present invention which particularly includes the structure of a vertical transistor, such as 21, which, in this embodiment, can be formed on top of a lateral transistor 11. As defined in claim 1, this combination of elements to form the transistor 21 can include a tower like gate pillar (e.g., 24) which includes a channel region 28c formed between impurity diffusion regions 28a and 28b (see page 10, second paragraph). A gate insulation film 23 is formed over the outer surface of the gate pillar, and a gate electrode film 22 is formed on the outer surface of the gate insulation film. As shown in the embodiment of Fig. 1, the gate electrode film is formed of a plurality of layers (e.g., 22a and 22b) "formed in order from said gate pillar, in the direction where said gate electrode film is formed."

With regard to this, it is noted that each of the embodiments of Figs. 1, 2, 5 and 7 includes this same combination of features of a tower like gate pillar 24, a gate